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1104E082

Candidate's Seat No :_____

M.Sc. (Sem.-IV) Examination

507

Electronic Science

Time : 3 Hours] **April-2017** **[Max. Marks : 70**

ELE-507 Integrated Circuit Technology

Instruction : **(1) Attempt all questions**

(2) Symbols used have their usual meanings

Q. 1 (a) What is metallurgical grade silicon (MGS)? Explain the method of electronic grade silicon (EGS) production. [7]

OR

(a) Derive an expression for maximum pull rate for silicon single crystal growth. Using a schematic diagram, briefly explain the Float Zone (FZ) crystal growth technique. [7]

(b) (i) Explain chemical mechanical polishing of silicon wafers. [3]

(ii) Segregation coefficient of oxygen in silicon is 0.25. Number of oxygen atoms per cm^3 in solid silicon ingots at 4% doping level is 1.3×10^{18}, find the concentration of oxygen in the crystal at a fraction solidification of 0.7 [4]

OR

(b) Define epitaxy. Explain growth kinetics of vapour phase epitaxy of silicon. [7]

Q. 2 (a) Write note on wet chemical etching and also discuss wet etching of silicon and silicon dioxide. [7]

OR

(a) Explain the Thermal Oxidation in details with diagram and its growth kinetics. [7]

(b) Write note on Photo-resist in Optical Lithography. [7]

OR

(b) Write in details how the pattern transfers in Optical Lithography. [7]

Q. 3 (a) Give the schematic of interstitial and interstitialcy models of diffusion. Obtain Fick's one dimensional diffusion equation for constant surface concentration [7]

OR

(a) Discuss the various designing considerations of VLSI packaging. [7]

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(b) List the desired properties of metallization in IC technology. Discuss the process of electromigration with Al metallization. How can it be reduced? [7]

OR

(b)Distinguish between diffusion and ion implantation. Explain (i) ion stopping mechanism and (ii) channeling process in a typical ion implantation. [7]

Q.4 (a) Discuss the basic fabrication process of Bipolar NPN Transistor giving suitable diagrams for each step. [7]

OR

(a) With the help of necessary diagrams discuss CMOS IC fabrication process sequence and isolation and latch-up consideration [7]

(b) Write fundamental the non-silicon GaAs- IC's fabrication technology and process sequence step by step. [7]

OR

(b)Explain the electrostatic discharge damage in VLSC circuits. Describe various methods to prevent it. [7]

Q. 5 Answer the following questions in brief : **[14]**

(i) State limitations of Czochralski (CZ) crystal growth technique.
(ii) Define segregation coefficient. State its importance.
(iii) Define junction spiking in case of top metallization.
(iv) Draw any two VLSI package types.
(v) Why Al is most preferred metal for top metallization in IC technology?
(vi) Why impurity carbon mostly occupies substitutional silicon site ?
(vii) Define getting. State its advantage.
(viii) What is meaning of class-100 clean room?
(ix) Which lithography technique has the highest resolution? Why?
(x) What do you mean by proximity and contact printing?
(xi) Name the common positive and negative electron resist.
(xii) Fabrication Facilities, pure water system used large quantities of ultraclean water. How much a specific resistivity of ultraclean water is considered to have a low ionic content.
(xiii) How "PUNCH-THRUOGH" condition occurs during channel doping in NMOS VLSI-tech?
(xiv) How is the Alpha particle induced soft errors? And how it can be reduced?

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