2404N329

Candidate's	Seat No	:

M.Sc. Semester-4 Examination

507

Electronics Science

Time: 2-30 Hours

April-2023

[Max. Marks: 70

Instructions:

- 1. Attempt all questions.
- 2. Assume data when necessary
- 3. Symbols used have their usual meanings.

Q-1 (A)	Explain the steps required for the silicon wafer shaping. Give details of the procedure of silicon wafer polishing. State its limitations.	7
(B)	What do you mean by metallurgical grade silicon? Using necessary diagram, explain the preparation of electronic grade silicon. OR	7
Q-1 (A)	Differentiate between Czochralski and float Zone methods of Silicon crystal growth. Discuss the Float Zone method (CZ) of Si-crystal growth.	7
(B)	Explain (i) segregation coefficient and effective segregation coefficient. (ii) Carbon and oxygen in grown silicon crystal	7
Q-2 (A)	Explain in detail, "wet etching technique". And also discuss, (1) silicon etching, (2) silicon oxidation etching.	7
(B)	Explain in detail, "Electron-beam lithography". OR	7
Q-2 (A)	Explain in detail, "pattern transfer in lithography".	7
(B)	Discuss in detail, " Photoresist materials of lithography". Explain the exposure-response curve of photoresist.	7
Q-3 (A)	Briefly explain vacancy model of diffusion. Explain the Fick's theory of diffusivity for constant surface concentration.	7
(B)	Explain the process of electromigration. How it can be reduced in metallization processes with aluminum?	7
	OR	
Q-3 (A)	Discuss different VLSI package types and their design considerations. Describe the die bonding process used in VLSI interconnects.	7
(B)	Distinguish between diffusion and ion implantation. Explain (i) ion stopping mechanism and (ii) channeling process in a typical ion implantation	7
Q-4 (A)	Explain the fabrication process of NMOS VLSI-IC Technology step-by-step. Explain the special case -(1) Isolation, (2) channel doping.	7
(B)	Discuss in detail, 'Fabrication process of GaAs VLSI-IC Technology' OR	7
Q-4 (A)	Explain the fabrication process of CMOS VLSI-IC Technology step-by-step. Explain the special case -(1) Isolation, (2) latch-up.	7
(B)	Discuss in detail, "Electrostatic Discharge Damage (EDD)". And write all the protection circuit mechanism.	7

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Q-5		Attempt any SEVEN questions from the following. Each carries TWO marks.
1	(a) (b)	Which type of wafer has only primary flat — {100} p-type {111} p-type {100} n-type {111} n-type
2	(a) (b) (c) (d)	In grown silicon crystal, the common impurities are carbon and oxygen, which most commonly occupy interstitial sites only substitutional sites only substitutional and interstitial sites respectively interstitial and substitutional sites respectively
3	(a) (b) (c) (d)	For heavy doping of silicon wafer, which method is suitable? Melt growth Diffusion Ion implantation Mechanical-chemical
4	(a) (b) (c) (d)	If the segregation coefficient $k_o < 1$, then Melt will be richer in impurity Crystal will be richer in impurity Point defects will be created in grown crystal Dislocations will be created in grown crystal
5	(a) (b) (c) (d)	Junction spiking is related to Metallization Ion impantation Diffusion Packaging
6	(a) (b) (c) (d)	The term <i>epoxy die bonding</i> is associated with Metallization Ion implantation Lithography Packaging
7		Explain how ion-beam lithography is better than electron-beam lithography?
8		P-glass deposition at lower temperatures becomes soft and flows upon heating. it provides smoother surface topology and isolation, but why we can't increase phosphorus content/concentration >8 wt% (weight percentage) in order to decrease flow angle?
Ģ	(a) (b) (c) (d)	The conductivity constant
1	Λ	What is the importance of LDD and DDD?

- 10
- Write how water can purify in the large quantity from variety of contaminations in the purification plant? 11
- What is called, "soft error", and how to stop this occurrence of soft error? 12