Seat No. : _____

# NA-101

**November-2013**

## S.Y.B.C.A. Sem.-III

## CC-201 : Computer Organization & Advanced Microprocessor

**Time : 3 Hours]** **[Max. Marks : 70**

**Instructions :** (1) Write each question on new page.
(2) Draw diagram wherever necessary.

1. (A) Answer the following questions :

(a) Explain Von Neumann architecture. **4**

(b) Explain Instruction Format with examples. **3**

**OR**

(a) Discuss CPU – Memory communication. **4**

(b) A clock signal has a frequency of 20 MHz with a duty cycle of 50%. Calculate its pulse width. **3**

(B) Answer briefly.

(a) Explain Device Controller. **4**

(b) Discuss CPU registers. **3**

**OR**

(a) Explain the steps required for instruction set design. **4**

(b) Write a note on BUS concept. **3**

2. (A) Answer the following questions :

(a) Convert following FPS number to decimal number : **4**

0 X C2508000 H

(b) Draw the block diagram and truth table of JK flip flop. **3**

**OR**

(a) Draw the block diagram and truth table of AND gate and EX-NOR gate. **4**

(b) Draw the block diagram and truth table of encoder. **3**

(B) Answer briefly.

(a) Draw the block diagram and truth table of NAND gate and EX-OR gate. **4**

(b) Convert following binary number in the single precision floating point standard : $(11.1)_2$ **3**

**OR**

(a) Draw the block diagram and truth table of Full Adder circuit. **4**

(b) Write a short note on floating point number. **3**

3. (A) Answer the following questions :

(a) Write a note on cache coherence. **4**

(b) Explain cache hit and cache miss. **3**

**OR**

(a) Write a note on Associative Memory. **4**

(b) Discuss any two memory parameters. **3**

(B) Answer briefly.

(a) Explain two write policies of cache. **4**

(b) Draw the block diagram of RAM and ROM chip of size 256 X 8. **3**

**OR**

(a) A computer has 32 bit main memory address and has 8 KB cache memory. The computer follows 4 way set-associative mapping. Each block size is 16 words. **4**

- Show the memory address format for set associative mapping.
- Show the memory address format for direct mapping.

(b) Discuss Instruction Prefetch and Write Buffer. **3**

4. (A) Answer the following questions :

(a) Write a note on mobile / tablet processors. **4**

(b) Discuss RICS processor. **3**

**OR**

(a) Explain EU and BIU of 8086 with diagram. **4**

(b) Write a note on Single Chip Micro Computers (Microcontrollers). **3**

(B) Answer briefly.

(a) Write a note on Intel core processors. **4**

(b) What is an interrupt ? List all software interrupts of 8086. **3**

**OR**

(a) Discuss the various flags of status registers. **4**

(b) Discuss Scalar, Superscalar and Array processors. **3**

5. Choose the correct option : **14**

(1) _____ register stores the results of the last processing step of the ALU.

(a) Memory address (b) Instruction

(c) Accumulator (d) Program counter

(2) _____ is a binary pattern design inside a microprocessor to perform a specific function.

(a) Fetch execute cycle (b) Logical operation

(c) Instruction (d) Data transfer operation

(3) MAR stands for _____.

(a) Memory Address Read (b) Memory Active Read

(c) Maximum Address Read (d) Memory Address Register

(4) _____ bit is used to represent negative sign in Signed Magnitude Form.

(a) 1 (b) – 1

(c) 0 (d) – 0

(5) _____ is a logical circuit that performs an addition operation on two binary digits.

(a) Half Adder (b) Flip-flop

(c) Full Adder (d) Decoder

(6) _____ is a device that accepts data from one of many input sources for transmission over a common shared line.

(a) Multiplexer (b) Decoder

(c) Demultiplexer (d) Encoder

(7) _____ is the access time taken by the first access in a series of accesses.

(a) Latency (b) Bandwidth

(c) Frequency (d) Cycle Time

(8) _____ technique is used to minimize the time a processor spends waiting for instruction to be fetched from memory.

(a) Instruction Prefetch (b) Read Buffer

(c) Write Buffer (d) None of these

(9) A memory unit accessed by the content is called _____ memory.

(a) Main (b) Cache

(c) Secondary (d) Associative

(10) Cycle Time = Access Time + _____.

(a) Recovery Time (b) Pulse Width

(c) Bandwidth (d) Duty Cycle

(11) RTL stands for _____.

(a) Register Temporary Language

(b) Register Transfer Language

(c) Random Temporary Language

(d) None of these

(12) _____ status pin decides the operating mode of 8086.

(a) MW/MR (b) MN/WR

(c) MN/MX (d) None of these

(13) In _____ addressing mode, operand is a part of the instruction.

(a) Direct (b) Immediate

(c) Indirect (d) None of these

(14) _____ is a digital computer built on a single chip and used for control application.

(a) Microprocessor (b) Microprogram

(c) Microcontroller (d) None of these