Seat No. : _____

DB-101

December-2021

BCA, Sem.-III

CC-201 : Computer Organization (New)

Time : 2 Hours]

[Max. Marks : 50

- **Instructions :** (1) All Questions in Section I carry equal marks.
 - (2) Attempt any **Two** questions in Section I.
 - (3) Question **5** in Section II is Compulsory.

Section – I

1.	(A)	(i) Draw logical diagram and truth table for half adder and JK flip flop.				
		(ii) Explain 4-bit synchronous binary counter. 5	;			
	(B)	(i) Define decoder and explain 3-to-8 line decoder. 5	j			
		 (ii) Draw logical diagram/graphical symbol and truth table for 4-1 line multiplexer, AND gate & NOT gate. 	;			
2.	(A)	Explain 4-bit binary adder circuit and error detection code.				
(B) Perform (i) Add +13 & -6 (ii) subtract +4 from +7 using 2's complem representation in 8 bit register. Also explain shift micro operation in brief.						
3.	(A)	Explain Instruction cycle with flowchart. Also explain direct and indirect addressing modes in brief. 10)			
	(B)	Explain 16-bit common bus system. 10	1			
4.	(A)	Explain handshaking method and programmed I/O mode of transfer.				
	(B)	Explain DMA with block diagram of DMA controller. 10)			
		Section – II				
5.	Sele	Select the correct option :				
	(1)	A circuit that performs the arithmetic addition of three input bits is called adder.				
		(a) Half Adder (b) Full Adder				
		(c) Multiplexer (d) Binary Adder				

P.T.O.

(2)		flip flop acts as a toggle	ch.					
	(a)	D	(b)	Т				
	(c)	SR	(d)	ЈК				
(3)	The	The 9's complement of a decimal number 718 is						
	(a)	281	(b)	282				
	(c)	283	(d)	284				
(4)	RTL stands for							
	(a)	Register Transfer Language						
	(b)	Register Transport Languag	je					
	(c)	Register Translate Language	e					
	(d)	Register Transform Langua	ge					
(5)	The memory read operation can be stated symbolically as							
	(a)	DR←MR[AR]	(b)	MR[AR]←DR				
	(c)	AR←MR[DR]	(d)	None of the above				
(6)	The operation code of an instruction specifies							
	(a) Type of operation to be performed							
	(b)	Memory address of operand	l					
	(c)	Register address of operand						
	(d)	None of the above						
(7)	is not an instruction code format.							
	(a)	Memory-reference	(b)	Register-reference				
	(c)	IO-Reference	(d)	None of these				
(8)	A computer goes to an interrupt cycle, when an interrupt flip-flop R is equal to							
	(a)	1	(b)	0				
	(c)	-1	(d)	None of the above				
(9)	determines which interrupt is to be served first when two or more requests are made simultaneously.							
	(a)	Interrupt priority	(b)	Interrupt occurrences order				
	(c)	Interrupt type	(d)	None of the above				
(10)	In I/O Bus and Interface Modules, interface may receive							
	(a)	Control command	(b)	Status command				
	(c)	IO command	(d)	All of the above				

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