Seat No. : _____

JG-122

June-2022

M.Sc., Sem.-II

409 : Physics

(Semiconductor Physics and Devices)

Time : 2 Hours]

[Max. Marks : 50

- **Instructions :** (1) All questions in Section I carry equal marks.
 - (2) Attempt any three questions in Section I.
 - (3) Questions in Section II is COMPULSORY.
 - (4) Symbols used have usual meanings.

SECTION – I

1.	(A)	Explain the formation of energy bands in semiconductor. Draw the energy band diagrams of metal, semiconductors and insulators.	7
	(B)	Prove that at any temperature, the location of Fermi level is at the centre of the forbidden gap in an intrinsic semiconductor.	7
2.	(A)	State and prove the law of mass action. Give its physical significance.	7
	(B)	Explain the formation of acceptor and donor states. Describe the effect of temperature on the Fermi level in p-type semiconductor.	7
3.	(A)	Draw the energy band diagram of a p-n junction at thermal equilibrium. Show that the location of the Fermi level is constant across the p-n junction.	7
	(B)	For an abrupt p-n junction assume a rectangular depletion region at thermal equilibrium. Obtain an expression of the built-in potential of the p-n junction.	7
4.	(A)	Obtain the Shokley equation of an ideal p-n junction diode.	7
	(B)	For an unbiased p-n junction, obtain an expression for depletion layer width.	7

- 5. (A) Define important JFET parameters and discuss the effect of temperature on drain current. A JFET has value of $g_{mo} = 3000 \mu S$. Determine the value of g_m at $V_{GS} = -4V$. Given that $V_{GS(off)} = -8V$. 7 (B) Give details of construction and working of Enhancement type N-channel MOSFET with suitable diagrams. Draw its output and transfer characteristics. 7 6. (A) Draw circuit of common gate amplifier using JFET and give its NORTON'S equivalent circuit. Write the expressions for its voltage gain, input and output resistances. The transconductance (gm) of a JFET Common Gate amplifier is 3000µS and load resistance is 10k ohm. Find voltage gain of amplifier. 7 7 (B) Write a note on Light Emitting Diode(LED). (A) Draw schematic diagram of 2-input TTL NAND gate and explain its working by 7. verifying the truth table. What should be done with floating input in TTL ICs ? 7 (B) Discuss worst case input and output profile voltages of standard TTL IC. Explain 7 the term "noise margin". 8. (A) Explain the concept of sourcing and sinking currents in TTL ICs ? Discuss standard loading rules for TTL ICs. 7 (B) Draw schematic diagram of 2-input CMOS-NAND gate and explain its working by verifying the truth table. Write the main characteristics of CMOS ICs. 7 **SECTION – II** 9. Attempt the following MCQs : 8 For a JFET $I_{Gss} = 10$ nA at $V_{Gs} = -10$ Volts and $V_{DS} = 0$ Volts. (1)The input resistance from Gate to Source is 100 MΩ (A) 1 MΩ **(B)**
 - $1000 \text{ M}\Omega$ (C) 10000 MΩ (D)

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- (2) An N-Channel Depletion MOSFET with positive V_{GS} is operational in
 - (A) The Depletion mode **(B)** The Enhancement mode
 - (C) Saturation mode (D) Cutoff mode
- (3) Three CMOS gates are cascaded. If each has got the propagation delay time of 20ns, what is the total propagation delay time?
 - (A) 6.66 ns (B) 20 ns
 - (C) 60 ns (D) 8 µs
- (4) What is the fanout of a standard TTL device driving a Low Power Schortky TTL Device (74LS)?
 - (A) 10 (B) 20
 - (C) 40 (D) 100
- (5) On which factors does the mobility of charge carriers depend?
 - Purity of the materials (B) Type of the charge carriers (A)
 - (D) All of the above (C) Temperature
- With increase in temperature of an n-type semiconductor, the Fermi level location (6) shifts towards the centre of the band gap due to
 - (A) Increase in the kT value
 - increase in the n_i having constant N (B)
 - (C) increase in the N_D having constant n_i
 - increase in the n_i and N_D both (D)
- If 10¹⁷ atoms·cm⁻³ antimony doped silicon possess the conductivity of (7)8.00 (Ω ·cm)⁻¹, then its electron mobility will be
 - (A) $500 \text{ cm}^2 \text{ V}^{-1}\text{S}^{-1}$ (B) $600 \text{ cm}^2 \text{V}^{-1}\text{S}^{-1}$
 - (D) 800 cm² V⁻¹S⁻¹ $700 \text{ cm}^2 \text{ V}^{-1} \text{S}^{-1}$ (C)
- (8) From the C-V characteristics of a p-n junction, one may estimate
 - (A) Space charge region width (B) Built-in potential
 - Charge carrier mobility (D) Band gap energy (C)